[0143] The controller **1000** may refer to a device for controlling an operation of the camera **1060**, at least one memory **1100** and/or **1101**, and the display **1200**. According to example embodiments, the controller **1000** may control an operation of a touch screen **1201**.

[0144] The controller **1000** may be embodied in including but not limited to, an integrated circuit, a motherboard, a system on chip (SoC), an application processor (AP), and/or a mobile AP.

[0145] Still referring to FIG. **13**, the controller **1000** may include a bus architecture **1010**, a central processing unit (CPU) **1020**, an image signal processor (ISP) **1030**, an encoder **800**A of FIG. **11** and/or **800**B of FIG. **12** (collectively, **800**), at least one memory controller **1040** and/or **1041**, and a display controller **1050**.

[0146] The bus architecture **1010** may be embodied in including but not limited to, an Advanced Microcontroller Bus Architecture (AMBA), an Advanced High-performance Bus (AHB), an Advanced Peripheral Bus (APB), an Advanced extensible Interface (AXI) or an Advanced System Bus (ASB); however, it is not limited thereto.

[0147] The CPU **1020** may control an operation of the image signal processor **1030**, the encoder **800**, the at least one memory controller **1040** and/or **1041**, and/or the display controller **1050** through the bus architecture **1010**.

[0148] The image signal processor **1030** may control a format transformation of image data outputted from the camera **1060**, a noise reduction of the image data, and an image enhancement of the image.

[0149] That is, for example, the image signal processor **1030** may transform first data having a first format outputted from the camera **1060** into second data having a second format. The first format may refer to a Bayer format, and the second format may refer to the YUV format, the YCbCr format, or the RGB format. The camera **1060** may include a complementary metal-oxide semiconductor (CMOS) image sensor chip.

[0150] It is shown in a non-limiting example embodiment of FIG. **1** that the image signal processor (ISP) **1030** is embodied in the controller **1000**, but the image signal processor **1030** may be placed in the controller **1000**, and the camera **1060** and may be embodied in an independent chip according to non-limiting example embodiments. According to example embodiments, the image signal processor **1030** may be placed in the camera **1060**. And, the CMOS image sensor chip and the image signal processor **1030** may be packaged in one package.

[0151] The encoder **800** of FIG. **13** may receive an input video signal and output an encoded bit stream BS through quantization/inverse quantization and transformation/inverse transformation operations. The encoder **800** may determine a quantization parameter appropriate for a block on which image processing is performed in the quantization/inverse quantization process, and perform the quantization/inverse quantization operation using the determined quantization parameter.

[0152] The encoder **800** may transmit the encoded bit stream BS to at least one memory **1100** and/or **1101** through at least one memory controller **1040** and/or **1041**.

[0153] The encoder **800** according to an example embodiment of inventive concepts may be an encoder which supports a H.264 video compression standard as shown in FIG. **11**, and may be an encoder which supports a High Efficiency Video Coding (HEVC) video compression standard as shown in FIG. **12**; however, it is not limited thereto.

[0154] At least one memory controller **1040** and/or **1041** may read encoded image data (for example, encoded bit stream) from at least one memory **1100** and/or **1101**. The encoded image data (for example, encoded bit stream) transmitted from the at least one memory controller **1040** and/or **1041** are decoded by a decoder (not shown), and the decoded image data may be transmitted to the display **1200** through the display controller **1050**.

[0155] A codec may include the encoder **800** and the decoder; however, an operation of the encoder **800** included in the codec is described in example embodiments of inventive concepts. The encoder **800** may perform a function of a compressor and a de-compressor.

[0156] At least one memory controller **1040** and/or **1041** may control a data access operation of at least one memory **1100** and/or **1101** according to a control of the CPU **1020**. The data access operation may include a write operation of writing data in the memory **1100** or **1101**, and a read operation of reading data from the memory **1100** or **1101**.

[0157] The at least one memory **1100** and/or **1101** may include a volatile memory and/or a non-volatile memory. The volatile memory may include but not limited to, a random access memory (RAM), a dynamic RAM (DRAM), a static RAM (SRAM), and/or a buffer memory.

[0158] The non-volatile memory may be embodied in a flash memory, a magnetic RAM (MRAM), a Spin-Transfer Torque MRAM, a ferroelectric RAM (FeRAM), a phase change RAM (PRAM), or a resistive RAM (RRAM).

[0159] The flash memory may be embodied in a NAND-type flash memory or a NOR-type flash memory for storing one or more bits.

[0160] That is, for example, the memory **1100** may be embodied in a DRAM, and the memory **1101** may be embodied in a flash-based memory. At this time, the memory controller **1040** may be embodied in a DRAM controller, and the memory **1041** may be embodied in a flash-based memory controller.

[0161] The flash-based memory may be embodied in a solid-state drive or solid-state disk (SSD), a multimedia card (MMC), an embedded MMC (eMMC), or a universal flash storage (EFS).

[0162] The display controller **1050** may transmit data outputted from the CPU **1020**, the encoder **800**, or the display controller **1050** to the display **1200** according to a control of the CPU **1020**.

[0163] The camera **1060** may include at least a CMOS image sensor chip. The CMOS image sensor chip may output image data corresponding to an optical image of a subject to the image signal processor **1030**. According to an example embodiment, the camera **1060** may output image data to the image signal processor **1030** through a Mobile Industry Processor Interface (MIPI) camera serial interface (CSI).

[0164] The display **1200** may display data output from the display controller **1050**. The touch screen **1201** may be used to select or to activate a graphic user interface (GUI) to be displayed on the display **1200**. That is, for example, the touch screen **1201** may generate a user touch input for controlling an operation of the controller **1000** and the user touch input may be supplied to the CPU **1020**.